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10/630,994	07/30/2003	Ken Gary Pomaranski	200311225-1	7732

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EXAMINER	
SAVLA, ARPAN P	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,994	POMARANSKI ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *23 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-15,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-15,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed February 23, 2006 in response to the Office action dated November 16, 2005. Claims 1, 4, 8, 12, and 18 have been amended. Claims 5 and 16 have been cancelled. Claims 1-4, 6-15, and 17-18 are pending in this application.

OBJECTIONS

Specification

1. In view of Applicant's amendment, the objections to the specification have been withdrawn.

Claims

2. In view of Applicant's amendment, the objections to **claims 1-2, 7, and 15** have been withdrawn.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

3. In view of Applicant's amendment, the 112 rejections to **claims 4 and 12** have been withdrawn.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. **Claims 12-17 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter**. The error handling code disclosed in **independent claim 12** is merely a computer program that is not embodied on a computer-readable medium needed to realize the computer program's functionality (such as the PDC unit). Therefore, the error handling code simply represents functional descriptive material.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-4, 6-7 are rejected under 35 U.S.C. 103(a) as being obvious over Jeddeloh et al. (U.S. Patent 5,862,314), hereafter "Jeddeloh-314", in view of Raynham et al. (U.S. Patent 5,774,647) and Faust et al. (U.S. Patent Application Publication 2003/0110426).

8. **As per claim 1**, Jeddeloh-314 discloses a method for persistently tracking volatile memory faults, the method comprising:

detecting a memory error relating to at least one dynamic random access memory (DRAM) unit on a particular memory module (col. 2, lines 51-55; col. 3, lines 3-12; and Fig. 2 element 50); *It should be noted that the error detecting occurs when the "error map" is being created in the factory that makes the memory module.*

and writing an entry pertaining to the memory error in non-volatile memory of a fault storage unit on the particular memory module (col. 2, lines 59-65; col. 3, lines 3-6; and Fig. 2, elements 52 and 54). *It should be noted that the "error map" is analogous to the "fault storage unit."*

Jeddeloh-314 does not expressly disclose the entry comprises a DRAM unit identifier, a start bit of the memory error, an end bit of the memory error, and tag bits indicating time of last failure and number of occurrences of failure.

Raynham discloses the entry comprises a DRAM unit identifier and tag bits indicating time of last failure and number of occurrences of failure (col. 10, lines 8-13 and 33-35; and col. 7, Table 2, the contents of bytes 24, 27, 41, 53, 54, and 118). *It should be noted that "byte 41 in Table 2" is analogous to the "DRAM unit identifier" and "byte 53 in Table 2" is analogous to "time of last failure."*

Jeddeloh-314 and Raynham are analogous art because they are from the same field of endeavor, that being logging errors in the non-volatile memory of memory modules.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Raynham's specific error log entry with Jeddeloh-314's entry on the non-volatile fault storage unit.

The motivation for doing so would have been to have management data containing identifying information about the DIMM, thus providing an efficient way to manage memory modules in a computer system (Raynham, col. 2, lines 32-33 and col. 7, lines 62-64).

The combination of Jeddeloh-314 and Raynham disclose a method for persistently tracking volatile memory faults, the method comprising:

detecting a memory error relating to at least one dynamic random access memory (DRAM) unit on a particular memory module;

writing an entry pertaining to the memory error in non-volatile memory of a fault storage unit on the particular memory module;

wherein the entry comprises a DRAM unit identifier and tag bits indicating time of last failure and number of occurrences of failure. *Please see citations directly above.*

The combination of Jeddeloh-314 and Raynham does not expressly disclose the entry comprises a start bit of the memory error and an end bit of the memory error.

Faust discloses the entry comprises a start bit of the memory error and an end bit of the memory error (paragraph 0027, lines 1-3 and 10-12; paragraph 0029, lines 4-6; paragraph 0040, lines 3-5; Fig. 2, element 230; Fig. 4, element 510). *It should be noted that "error log" is analogous to "entry", "storage device 230" is analogous to "fault storage unit", and the "defective bit identification information" contains the "start bit of the memory error and an end bit of the memory error." It should also be noted that in a single bit error, the start bit of the memory error and the end bit of the memory error are the same bit.*

The combination of Jeddeloh-314/Raynham and Faust are analogous art because they are from the same field of endeavor, that being logging errors in the non-volatile memory of memory modules.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Faust's defective bit identification information within Jeddeloh-314/Raynham's entry on the non-volatile fault storage unit.

The motivation for doing so would have been to more easily repair and recycle memory modules due to the identification of the defective memory elements being stored on the memory module itself (Faust, paragraph 0042, lines 4-7).

Therefore, it would have been obvious to combine Jeddeloh-314, Raynham, and Faust for the benefit of obtaining the invention in claim 1.

9. **As per claim 2**, the combination of Jeddeloh-798/Raynham/Faust discloses the particular memory module comprises a particular dual in-line memory module (DIMM) of a plurality of DIMMs in a memory system (Jeddeloh-798, col. 2, lines 49-51 and Fig. 1, element 12).

10. **As per claim 3**, the combination of Jeddeloh-798/Raynham/Faust discloses determining a scope of the detected memory error (Faust, paragraph 0034, lines 1-4; paragraph 0036, lines 1-7; Fig. 3, elements 330, 350, and 360). *It should be noted that when taking the broadest reasonable interpretation of the claim language it is clear that the limitations of the claim do not specify what determines the specific scope of the detected memory error. Faust assigns a defective tag to memory modules when the*

number of errors exceed a threshold, thus Faust discloses determining a scope of the detected memory error.

11. **As per claim 4**, the combination of Jeddeloh-798/Raynham/Faust discloses the scope of the memory error is determined by using a history of faults associated with the particular memory module (Faust, paragraph 0034, lines 1-4; paragraph 0036, lines 1-6; Fig. 3, elements 330 and 350). *It should be noted that "quantity/number of errors" is analogous to "history of faults."*

12. **As per claim 6**, the combination of Jeddeloh-798/Raynham/Faust discloses reading the entry from the non-volatile memory of the fault storage unit (Jeddeloh-798, col. 3, lines 27-30 and Fig. 2, element 56); *It should be noted that when "the processor in the memory controller receives a copy of the error map" it is analogous to "reading the entry from the non-volatile memory of the fault storage unit."*

and removing memory bits associated with the memory error from a set of usable memory (Jeddeloh-798, col. 3, lines 52-63 and Fig. 2, element 60). *It should be noted that remapping error bits is virtually removing bits from defective portions of memory by re-addressing the bits to working portions of memory, thus, removing the entire portion of defective memory as far as the system processor is concerned.*

13. **As per claim 7**, the combination of Jeddeloh-798/Raynham/Faust discloses removing memory bits associated with the memory error from a set of usable memory while the particular memory module remains online (Jeddeloh-798, col. 3, lines 52-63; col. 4, lines 49-57; and Fig. 2, element 60). *It should be noted that since the creating and storing of the remapping table is transparent to the processor, the memory module*

continues to stay online while the error bits are remapped. Also, see citation note for claim 6 above in regards to remapping error bits.

14. Claims 8, 10, 11, and 18 are rejected under 35 U.S.C. 103(a) as being obvious over Jeddeloh et al. (U.S. Patent 6,052,798), hereafter "Jeddeloh-798," in view of Raynham and Faust.

15. **As per claim 8**, Jeddeloh-798 discloses a memory module that persistently tracks volatile memory faults, the memory module comprising:

a plurality of dynamic random access memories (DRAMs) (col. 2, lines 61-63 and Fig. 1, element 12);

and a fault storage unit including non-volatile memory configured to store entries pertaining to faults in the plurality of DRAMs on that memory module (col. 2, line 59 – col. 3, line 6 and Fig. 1, elements 16 and 18). *It should be noted that the error detecting occurs when the "error map" is being created in the factory that makes the memory module.*

Jeddeloh-798 does not expressly disclose each said entry comprises a DRAM unit identifier, a start bit of the memory error, an end bit of the memory error, and tag bits indicating time of last failure and number of occurrences of failure.

Raynham discloses each said entry comprises a DRAM unit identifier and tag bits indicating time of last failure and number of occurrences of failure (col. 10, lines 8-13 and 33-35; and col. 7, Table 2, the contents of bytes 24, 27, 41, 53, 54, and 118). *It should be noted that "byte 41 in Table 2" is analogous to the "DRAM unit identifier" and "byte 53 in Table 2" is analogous to "time of last failure."*

Jeddeloh-798 and Raynham are analogous art because they are from the same field of endeavor, that being logging errors in the non-volatile memory of memory modules.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Raynham's specific error log entry with Jeddeloh-798's entry on the non-volatile fault storage unit.

The motivation for doing so would have been to have management data containing identifying information about the DIMM, thus providing an efficient way to manage memory modules in a computer system (Raynham, col. 2, lines 32-33 and col. 7, lines 62-64).

The combination of Jeddeloh-798 and Raynham disclose a memory module that persistently tracks volatile memory faults, the memory module comprising:

a plurality of dynamic random access memories (DRAMs);

a fault storage unit including non-volatile memory configured to store entries pertaining to faults in the plurality of DRAMs on that memory module;

wherein each said entry comprises a DRAM unit identifier and tag bits indicating time of last failure and number of occurrences of failure. *Please see citations directly above.*

The combination of Jeddeloh-798 and Raynham does not expressly disclose each said entry comprises a start bit of the memory error and an end bit of the memory error.

Faust discloses each said entry comprises a start bit of the memory error and an end bit of the memory error (paragraph 0027, lines 1-3 and 10-12; paragraph 0029, lines 4-6; paragraph 0040, lines 3-5; Fig. 2, element 230; Fig. 4, element 510). *It should be noted that "error log" is analogous to "entry", "storage device 230" is analogous to "fault storage unit", and the "defective bit identification information" contains the "start bit of the memory error and an end bit of the memory error." It should also be noted that in a single bit error, the start bit of the memory error and the end bit of the memory error are the same bit.*

The combination of Jeddeloh-798/Raynham and Faust are analogous art because they are from the same field of endeavor, that being logging errors in the non-volatile memory of memory modules.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Faust's defective bit identification information within Jeddeloh-798/Raynham's entry on the non-volatile fault storage unit.

The motivation for doing so would have been to more easily repair and recycle memory modules due to the identification of the defective memory elements being stored on the memory module itself (Faust, paragraph 0042, lines 4-7).

Therefore, it would have been obvious to combine Jeddeloh-798, Raynham, and Faust for the benefit of obtaining the invention in claim 8.

16. **As per claim 10**, the combination of Jeddeloh-798/Raynham/Faust discloses an entry stored in the non-volatile memory of the fault storage unit includes a DRAM identifier and a range of bits (Raynham, col. 9, lines 5-7; Table 2, the contents of bytes

41, 42, and 43; Table 4, the contents of the "bits" line). *It should be noted that byte 41 in Table 2 is analogous to the "DRAM unit identifier." It should also be noted that the "two-byte time stamp" indicating when the DIMM was turned comprises a range of bits (as seen in Table 4).*

17. **As per claim 11**, the combination of Jeddeloh-798/Raynham/Faust discloses the memory module comprises a dual in-line memory module (DIMM) (Jeddeloh-798, col. 2, lines 57-59 and Fig. 1, element 12).

18. **As per claim 18**, Jeddeloh-798 discloses a memory system comprising:

means for reading data from and writing data to volatile memory units on a plurality of memory modules (col. 4, lines 26-34; col. 5, lines 53-59; and Fig. 1, element 20); *It should be noted that page 7, lines 5-6 of Applicant's specification defines means as a memory controller.*

and means for reading error entries from and writing error entries to a non-volatile fault storage unit on each memory module (col. 3, lines 36-39 and Fig. 1, element 36). *It should be noted that page 8, lines 13-15 of Applicant's specification defines means as a memory error interface. Jeddeloh-798's "memory controller processor" is equivalent to Applicant's "memory error interface."*

Jeddeloh-798 does not expressly disclose an error entry comprises a DRAM unit identifier, a start bit of the memory error, an end bit of the memory error, and tag bits indicating time of last failure and number of occurrences of failure.

Raynham discloses an error entry comprises a DRAM unit identifier and tag bits indicating time of last failure and number of occurrences of failure (col. 10, lines 8-13

and 33-35; and col. 7, Table 2, the contents of bytes 24, 27, 41, 53, 54, and 118). *It should be noted that "byte 41 in Table 2" is analogous to the "DRAM unit identifier" and "byte 53 in Table 2" is analogous to "time of last failure."*

Jeddeloh-798 and Raynham are analogous art because they are from the same field of endeavor, that being logging errors in the non-volatile memory of memory modules.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Raynham's specific error log entry with Jeddeloh-798's entry on the non-volatile fault storage unit.

The motivation for doing so would have been to have management data containing identifying information about the DIMM, thus providing an efficient way to manage memory modules in a computer system (Raynham, col. 2, lines 32-33 and col. 7, lines 62-64).

The combination of Jeddeloh-798 and Raynham disclose a memory system comprising:

means for reading data from and writing data to volatile memory units on a plurality of memory modules;

and means for reading error entries from and writing error entries to a non-volatile fault storage unit on each memory module,

wherein an error entry comprises a DRAM unit identifier and tag bits indicating time of last failure and number of occurrences of failure. *Please see citations directly above.*

The combination of Jeddeloh-798 and Raynham does not expressly disclose an error entry comprises a start bit of the memory error and an end bit of the memory error.

Faust discloses an error entry comprises a start bit of the memory error and an end bit of the memory error (paragraph 0027, lines 1-3 and 10-12; paragraph 0029, lines 4-6; paragraph 0040, lines 3-5; Fig. 2, element 230; Fig. 4, element 510). *It should be noted that "error log" is analogous to "entry", "storage device 230" is analogous to "fault storage unit", and the "defective bit identification information" contains the "start bit of the memory error and an end bit of the memory error." It should also be noted that in a single bit error, the start bit of the memory error and the end bit of the memory error are the same bit.*

The combination of Jeddeloh-798/Raynham and Faust are analogous art because they are from the same field of endeavor, that being logging errors in the non-volatile memory of memory modules.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Faust's defective bit identification information within Jeddeloh-798/Raynham's entry on the non-volatile fault storage unit.

The motivation for doing so would have been to more easily repair and recycle memory modules due to the identification of the defective memory elements being stored on the memory module itself (Faust, paragraph 0042, lines 4-7).

Therefore, it would have been obvious to combine Jeddeloh-798, Raynham, and Faust for the benefit of obtaining the invention in claim 18.

19. Claim 9 is rejected under 35 U.S.C. 103(a) as being obvious over Jeddeloh-798 in view of Raynham and Faust as applied to claim 1 above, and in further Galanti (U.S. Patent 3,693,052).

20. **As per claim 9**, the combination of Jeddeloh-798/Raynham/Faust discloses interface circuitry configured to provide read and write access by a memory error interface unit to the non-volatile memory of the fault storage unit (Jedelloh-798, col. 3, lines 36-39 and Fig. 1, elements 16 and 36). *It should be noted that for there to be any connection between the memory error interface unit and the non-volatile memory of the fault storage unit (or any computer units in general) it is inherently required there be "interface circuitry." The bus line arrows between element 18 and element 20 in Fig. 1 are being citied even though they are not labeled as an element.*

The combination of Jeddeloh-798/Raynham/Faust does not expressly disclose that the memory error interface unit is on a circuit board.

Galanti discloses a circuit board (col. 2, lines 45-46 and Fig. 1, element 10).

The combination of Jeddeloh-798/Raynham/Faust and Galanti are analogous art because they are from the same field of endeavor, that being electrical circuitry.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to lay Jeddeloh-798/Raynham/Faust's memory error interface unit on Galanti's circuit board.

The motivation for doing so would have been to make it economically possible to mass produce electronic apparatuses, save space and weight, and substantially increase the reliability of electronic equipment (Galanti, col. 1, lines 22-26).

Therefore, it would have been obvious to combine Galanti with the combination of Jeddeloh-798/Raynham/Faust for the benefit of obtaining the invention as specified in claim 9.

Response to Arguments

21. Applicant's arguments with respect to **claims 1-4, 6-11, and 18** have been considered but are moot in view of the new ground(s) of rejection.

1st POINT OF ARGUMENT

Applicant's Argument:

22. Applicant argues in the first full paragraph of page 10, the second full paragraph of page 11, and the second full paragraph of page 14 filed on February 23, 2006 that "Jeddeloh-314 neither teaches nor suggests writing entries into the non-volatile memory of the memory module which identify a failed bit range and which include tag bits indicating time of last failure and number of occurrences of failure."

Examiner's Response:

23. The Examiner agrees that Jeddeloh-314 fail to teach the limitations recited in the now amended claim 1. However, the Examiner would like to point out that claim 1 as originally presented in the instant application did not require these limitations and therefore applicant's claims were naturally interpreted outside of these limitations. Per Applicant's amendment, the Examiner has now limited the scope of these claims to now include the aforementioned limitations. Please see the rejection provided above.

2ND POINT OF ARGUMENT

Applicant's Argument:

24. Applicant argues in second full paragraph of page 10, the third full paragraph of page 11, and third full paragraph of page 14 filed on February 23, 2006 that "Raynham-647 and Galanti also do not teach writing entries into the non-volatile memory of the memory module which identify a failed bit range and which include tag bits indicating time of last failure and number of occurrences of failure."

Examiner's Response:

25. The Examiner agrees with Applicant's position that Galanti does not disclose the limitations recited above and again points Applicant's attention to the fact that claim 1 as originally presented in the instant application did not require these limitations and therefore Applicant's claims were naturally not interpreted as being limited by these limitations. Per Applicant's amendment, the Examiner has now limited the scope of these claims to now include the aforementioned limitations. Please see the rejection provided above. Furthermore, the Examiner respectfully disagrees with Applicant's position that Raynham does not teach the limitation of "writing entries into the non-volatile memory of the memory module which include tag bits indicating time of last failure and number of occurrences of failure..." and respectfully request that Applicant consider the position that Table 2, byte 41 (DRAM identifier), Table 2, byte 53 (time of last failure), and Table 2, bytes 24 and 27 (number of occurrences of failure) taught by Raynham meet the above recited limitations, as noted by the Examiner in the rejection above.

26. Also, the Examiner would like to note that Applicant's arguments presented on pages 10-14 of the amendment are all drawn to, what Applicant calls, a failure of the cited references to teach "writing entries into the non-volatile memory of the memory module which identify a **failed bit range** and include tag bits indicating time of last failure and number of occurrences of failure." However, the Examiner would like to draw Applicant's attention to the fact that Applicant's independent claims, as amended, fail to recite the limitation of "a failed bit range" but rather recite "a start bit of the memory error and an end bit of the memory." The Examiner would like to emphasize that "a start bit of the memory error and an end bit of the memory" represents a very different limitation than "a failed bit range." Accordingly, these claims have been considered by the Examiner to contain a new limitation not earlier presented and have been interpreted differently than the originally presented claims.

27. Applicant's amendments filed on February 23, 2006 with respect to **claims 12-17** have overcome the cited prior art, therefore, the 103 rejections to these claims have been withdrawn. However, Applicant's amendments to **claims 12-17** have resulted in a 101 rejection as discussed above.

Accordingly, Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

Allowable Subject Matter

28. In view of Applicant's amendment, the 103 rejections to **Claims 12-17** would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 101, set forth in this Office action.

29. The primary reasons for allowance of **claims 12-17** in the application is the combination with the inclusion in these claims that "**error handling code including instructions to write entries relating to detected memory errors into the non-volatile fault storage unit and to read said entries from the non-volatile fault storage unit, wherein each said entry comprises a memory unit identifier, a start bit of a memory error, an end bit of the memory error, and tag bits indicating time of last failure and number of occurrences of failure.**" The prior art of record neither anticipates nor renders obvious the above recited combination.

30. As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the MPEP.

Claims Rejected in the Application

31. Per the Office action, **claims 1-11** have received a second action on the merits and are subject of a second action final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 6,976,197 discloses an apparatus and method for error logging on a memory module, such as a DIMM (U.S. Patent of Faust et al. 2003/0110426).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Arpan Savla
Assistant Examiner
Art Unit 2185
April 27, 2006

DONALD SPARKS
SUPERVISORY PATENT EXAMINER